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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,729	05/25/2004	Akiko F. Balchiunas	BUR920040137US1	3728

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EXAMINER	
TANG, MINH NHUT	
ART UNIT	**PAPER NUMBER**
2829	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,729	BALCHIUNAS, AKIKO F.	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,22-28 and 30-36* is/are rejected.

7)☒ Claim(s) *8-21 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 8-21 and 29 are objected to because of the following informalities:

a/ in claim 8, lines 13-14, "said additional groups" (plural) referred to "an additional group" (singular) recited previously; therefore "said additional groups" should be -- said additional group --.

b/ in claim 15, lines 13-14 and 16, "said additional groups" (plural), "said additional failing groups" (plural) referred to "an additional group" (singular), "an additional failing group" (singular) recited previously; therefore "said additional groups", and "said additional failing groups" should be -- said additional group --, and -- said additional failing group --, respectively.

c/ in claim 29, line 9, "and" should be deleted.

d/ claims 9-14 and 16-21 are objected since they depend on objected base claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 22-28, and 30-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Debenham (U.S.P. 5,764,650).

As to claims 1 and 30, Debenham discloses, in Figs. 1-3, a method for testing integrated circuit devices (50, 52) after manufacture, said method comprising: testing (see, for example, step 104 in Fig. 3) a group of devices (50, 52) to produce a failing group of devices (i.e., a number of identify failures in semiconductor devices 50 and 52, hereinafter, failure devices) that failed said testing (step 104), wherein said devices in said failing group (failure devices) are identified by type of failure (for example, location of bad memory cells); and retesting (see, for example, step 122 in Fig. 3) only devices in said failing group (failure devices) that have a type of defect (i.e., failures) approved for retesting.

As to claims 2 and 31, Debenham discloses in Figs. 1-3, retesting (see, for example, steps 122, 142) devices (failure devices) having types of defects (see, for example, column 1, lines 34-45) associated with testing.

As to claims 3, 24 and 32, Debenham discloses in Figs. 1-3, said testing process comprises probe type testing (using probes 82 shown in Fig. 2).

As to claims 4, 25 and 33, Debenham discloses in Figs. 1-3, said devices (50, 52) comprise integrated circuit chips (package chips and chips or dice on wafer).

As to claims 5 and 34, Debenham discloses in Figs. 1-3, said retesting process (steps 122 and/or 142) is optimized by only retesting devices in said failing group (failure devices) that have said type of defect (failures) approved for retesting.

As to claims 6 and 35, Debenham discloses in Figs. 1-3, a listing of types of defects (i.e., number of failures) approved for retesting comprises an optimized retest table (i.e., a record of the number of failures).

As to claims 7 and 36, Debenham discloses in Figs. 1-3, said type of defect (failures) approved for retesting is based upon previously acquired statistics of previous testing of the same type of device (see column 7, lines 50-56).

As to claim 22, Debenham discloses, in Figs. 1-3, a system (10) for testing integrated circuit devices (50, 52) after manufacture, said system (10) comprising: a tester (46) adapted to test devices (50, 52); a database (provided by the testing controller 90) comprising types of defects (for example, location of bad memory cells, failed bits, bad contacts between probes and the devices, etc.) approved for retesting, wherein said types of defects (failures) approved for retesting are based upon previously acquired statistics of which types of failures have retest passing rates, after initially failing testing, above a predetermined threshold; and a processor (12) in communication with said tester (46) and said database (90), wherein said processor (12) is adapted to direct said tester (46) to test a group of devices (50, 52) to produce a failing group of devices (i.e., a number of identify failures in semiconductor devices 50 and 52, hereinafter, failure devices) that failed said testing, wherein said processor (12) is further adapted to direct said tester (46) to retest only devices in said failing group (failure devices) that have one of said types of defects (failures) approved for retesting.

As to claim 23, Debenham discloses in Figs. 1-3, said database (90) includes types of defects (failures) associated with testing errors (i.e., bad connection between a lead finger and a probe or other test device) within said types of defects (failures) approved for retesting.

As to claim 26, Debenham discloses in Figs. 1-3, said processor (12) optimizes said retesting of said devices (failure devices) when controlling said tester (46).

As to claim 27, Debenham discloses in Figs. 1-3, said database (90) comprises an optimized retest table (i.e., a record of the number of failures).

As to claim 28, Debenham discloses in Figs. 1-3, said statistics of said types of defects (failures) relate to the same type of device being tested.

Allowable Subject Matter

4. Claims 8-21 and 29 are allowed over the art of record.

5. The following is a statement of reasons for the indication of allowable subject matter:

Claim 8 recites, inter alia, a method for testing integrated circuit devices after manufacture, said method comprising analyzing said devices in said retested passing group to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure; evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce a listing of types of defects approved for retesting; testing an additional failing group of devices that is different from said initial group of devices to produce an additional failing group of devices that failed said testing of said additional group; and retesting only devices in said additional failing group that have one of said types of defects approved for retesting.

Claim 15 recites, inter alia, a method for testing integrated circuit devices after manufacture, said method comprising analyzing said devices in said retested passing

group to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure; evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce a listing of types of defects approved for retesting; testing an additional failing group of devices that is different from said initial group of devices to produce an additional failing group of devices that failed said testing of said additional group; identifying types of devices having a predetermined reduced demand; and retesting only devices in said additional failing group that have one of said types of defects approved for retesting and that are not said types of devices for which there is said predetermined reduced demand.

Claim 29 recites, inter alia, a system for testing integrated circuit devices after manufacture, said system comprising means for analyzing said devices in said retested passing group to produce statistics regarding the likelihood that a failing device will pass said retesting according to said type of failure; means for evaluating said statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce a listing of types of defects approved for retesting; means for testing an additional failing group of devices that is different from said initial group of devices to produce an additional failing group of devices; and means for retesting only devices in said additional failing group that have one of said types of defects approved for retesting.

Claims 9-14 and 16-21 are allowed due to their dependency.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

It is noted that claims 8, 15 and 29 should be amended to overcome the objections set forth above.

Response to Arguments

6. Applicant's arguments filed on November 03, 2006 have been fully considered but they are not persuasive:

With respect to claims 1, 22 and 30, Applicants, in the Remarks pages 12 and 14, asserted that Debenham does not disclose resting only devices in said failing group that have a type of defect approved for retesting, step 122 in Fig. 3 of Debenham does not disclose retesting only devices in the failing group that have a type of defect approved for retesting, but rather retesting devices that have more than a specified number of failures. The Examiner respectfully disagrees. Debenham discloses "The test may involve determining a number of failures (F), for example, failed bits, in a semiconductor device" (column 8, lines 16-18), "if there are no fail bits F, the semiconductor device passes the hot sort test. Otherwise, the semiconductor device fails the hot sort test" (column 8, lines 24-26), "If F [i.e., fail bits] is not less than X1 (i.e., F is within the third number set), then the semiconductor device may be retested, such as in another hot sort, as is illustrated in box 122" (column 9, lines 7-9), "A method of determining the threshold may include performing tests on numerous semiconductor devices and creating a record of the number of failures, and retesting the semiconductor devices and creating a record of the number of failures determined in the retest"

(column 9, lines 23-27). Therefore, the semiconductor devices that have at least one of identified failures, for example, fail bits, are retested in step 122 and thus Debenham does disclose retesting only devices in the failing group that have a type of defect approved for retesting.

Prior Art Of Record

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Beffa 5,867,505 Method And Apparatus For Testing An Integrated Circuit Including The Step/Means For Storing An Associated Test Identifier In Association With Integrated Circuit Identifier For Each Test To Be Performed On The Integrated Circuit.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha T. Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Minh Tang

MINH NHUT TANG
PRIMARY EXAMINER

01/16/07